REMARKS

Applicant would like to thank the Examiner for his thorough examination of the present application and for indicating the patentability of remaining Claims 9-16, 19-26 and 29-32. The various informalities as also helpfully pointed out by the Examiner have been addressed in the amendments to the specification and the title has been amended as helpfully suggested by the Examiner. The inadvertent errors referring to FIGS. 5 and 6 have been corrected. It is noted that reference sign 26 is shown in FIG. 3E. A replacement Abstract is also submitted.

Applicants noticed that the Official Action included no confirmation of consideration of the Information Disclosure Statement submitted to the USPTO on August 20, 2003. In case these materials have become separated from the Examiner's file, enclosed is a copy of the originally filed IDS, cited references, and postcard indicating receipt by the U.S. Patent and Trademark Office.

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. If, after reviewing this Response, there are any remaining informalities which need to be resolved before the

application can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, WASHINGTON, D.C. 20231, on this 4th day of November, 2003.

METHOD OF FABRICATING PRESSURE SENSOR MONOLITHICALLY INTEGRATED

Abstract of the Disclosure

A method of making a monolithically integrated pressure sensor includes making a cavity in the semiconductor substrate. This may be formed by plasma etching the front side or the back side of the silicon wafer to cut a plurality of trenches or holes deep enough to extend for at least part of its thickness into a doped buried layer of opposite type of conductivity of the substrate and of the epitaxial layer grown over it. The method may also include electrochemically etching through such trenches, and the silicon of the buried layer with an electrolytic solution suitable for selectively etching the doped silicon of the opposite type of conductivity, thereby making the silicon of the buried layer porous. The method may also include oxidizing and leaching away the silicon so made porous.